

FIG. 1

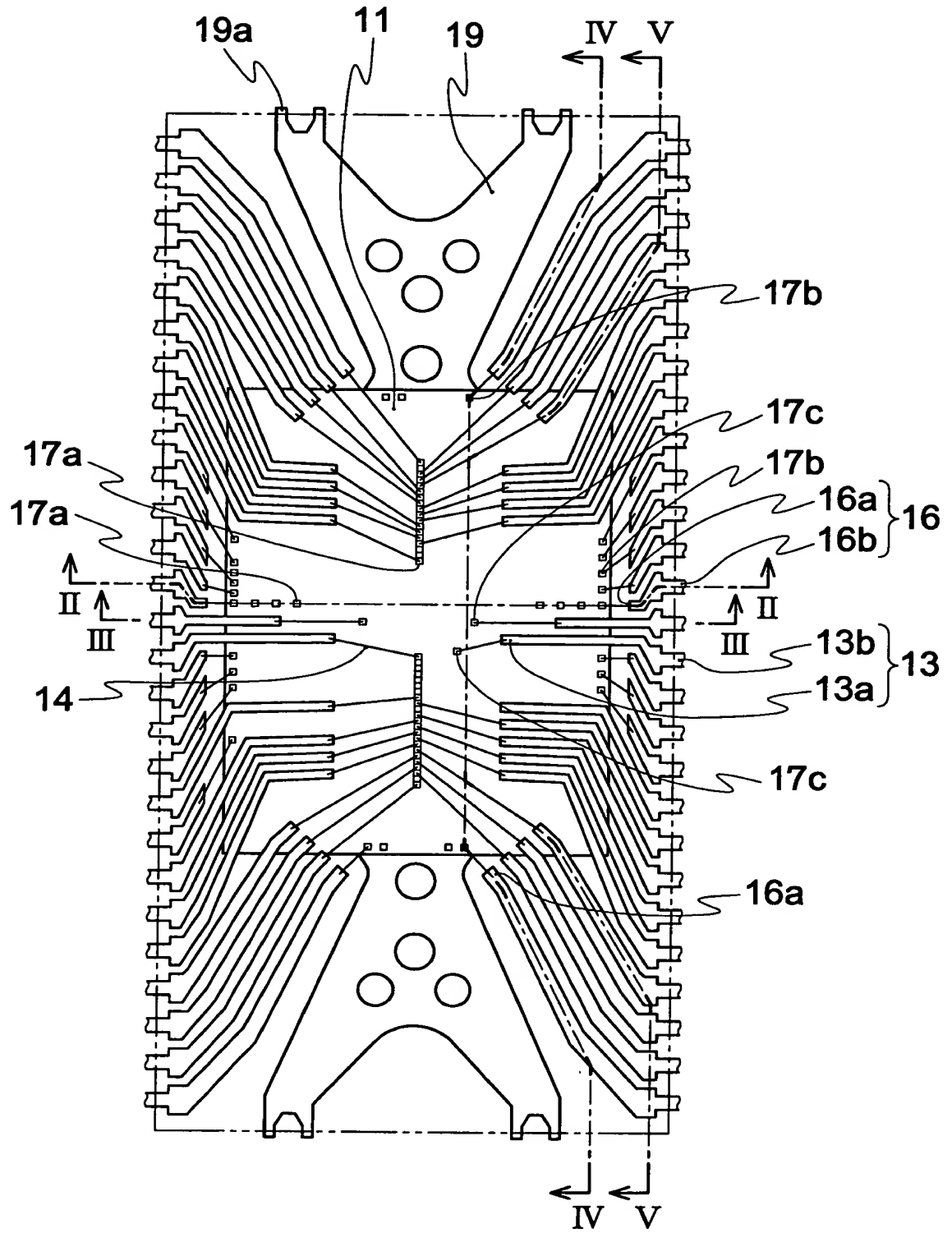


FIG. 2

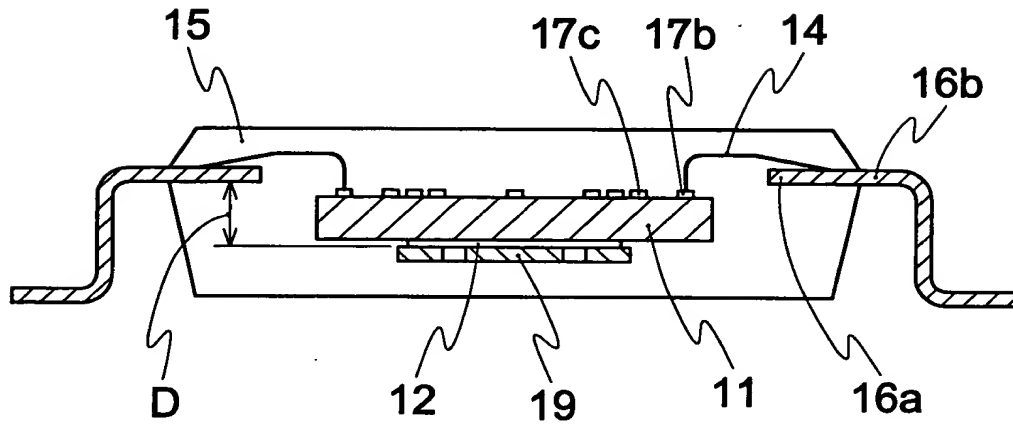


FIG. 3

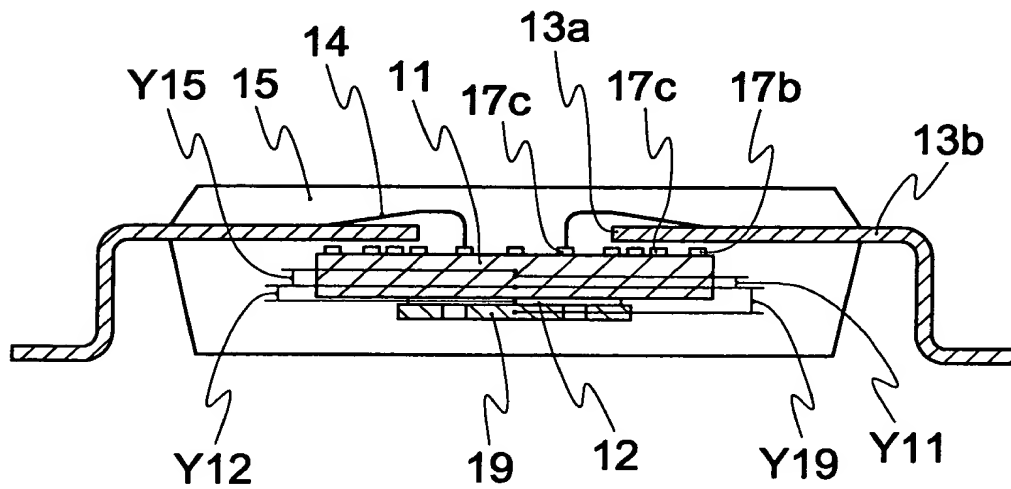


FIG. 4

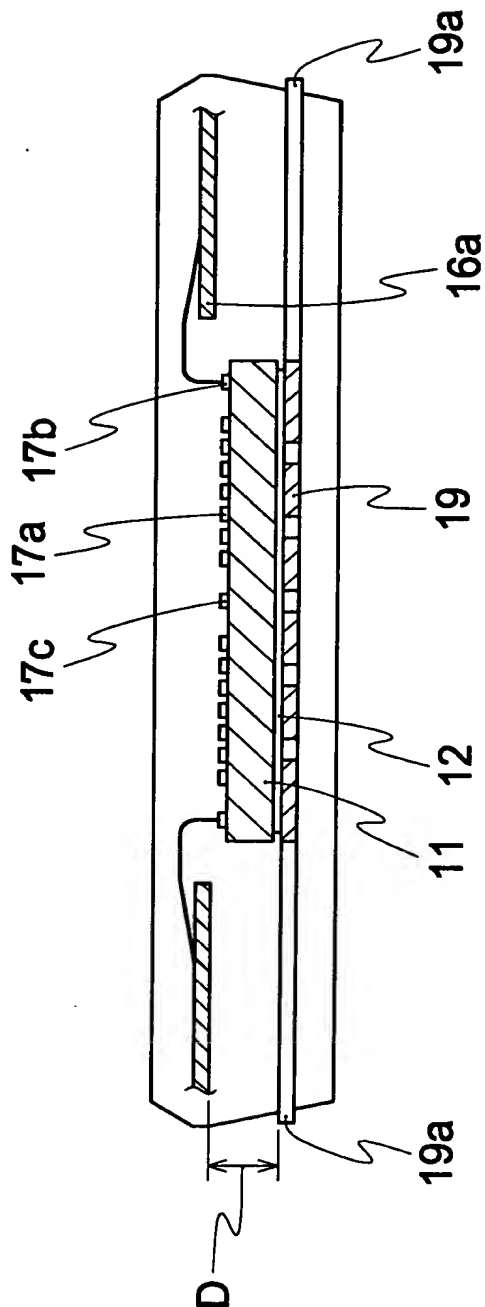


FIG. 5

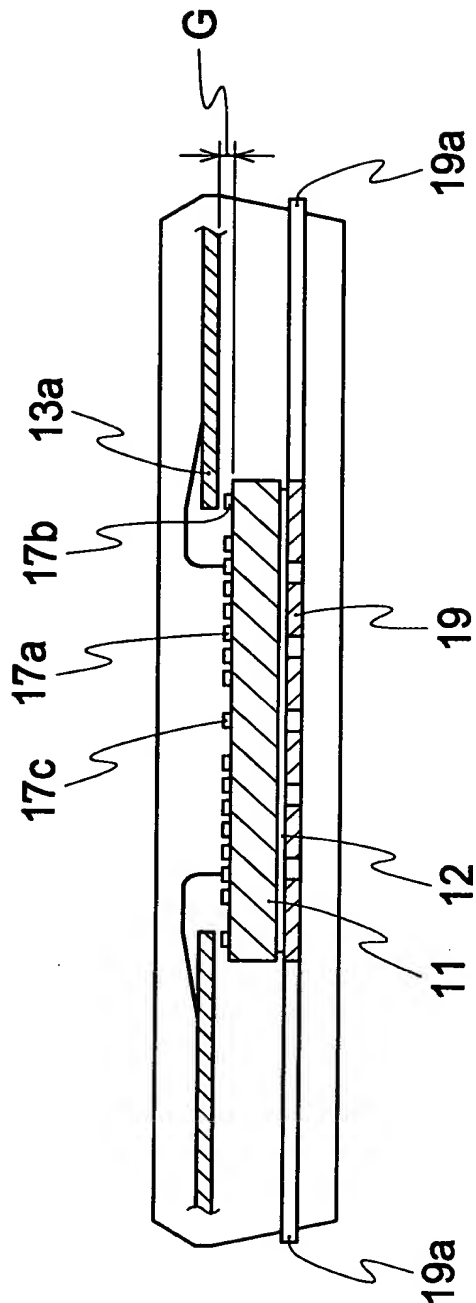


FIG. 6

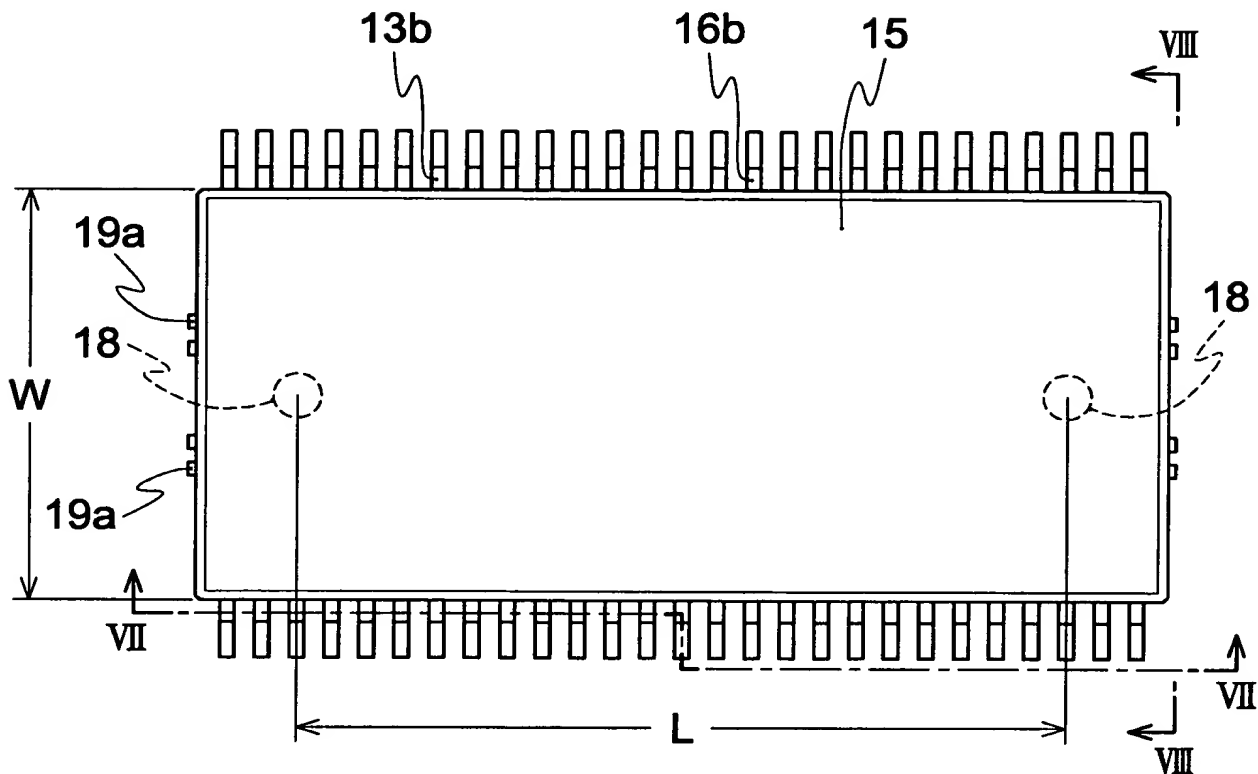


FIG. 7

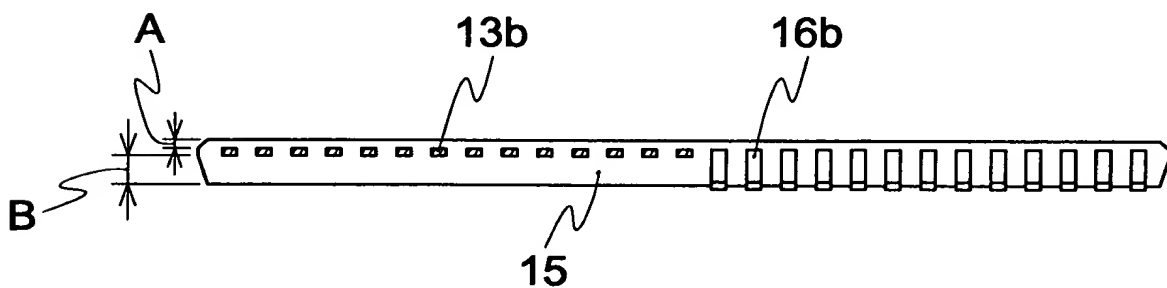


FIG. 8

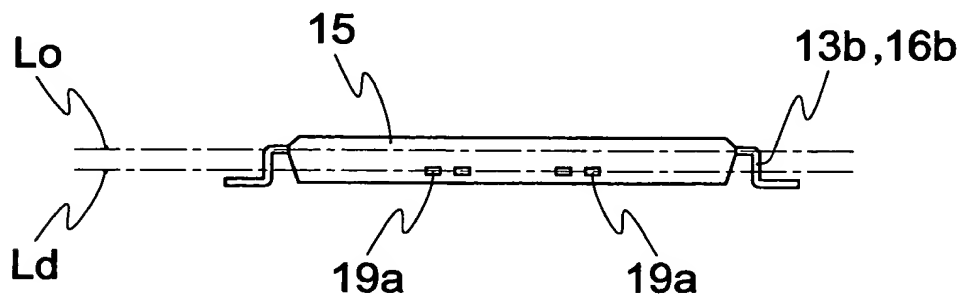


FIG. 9

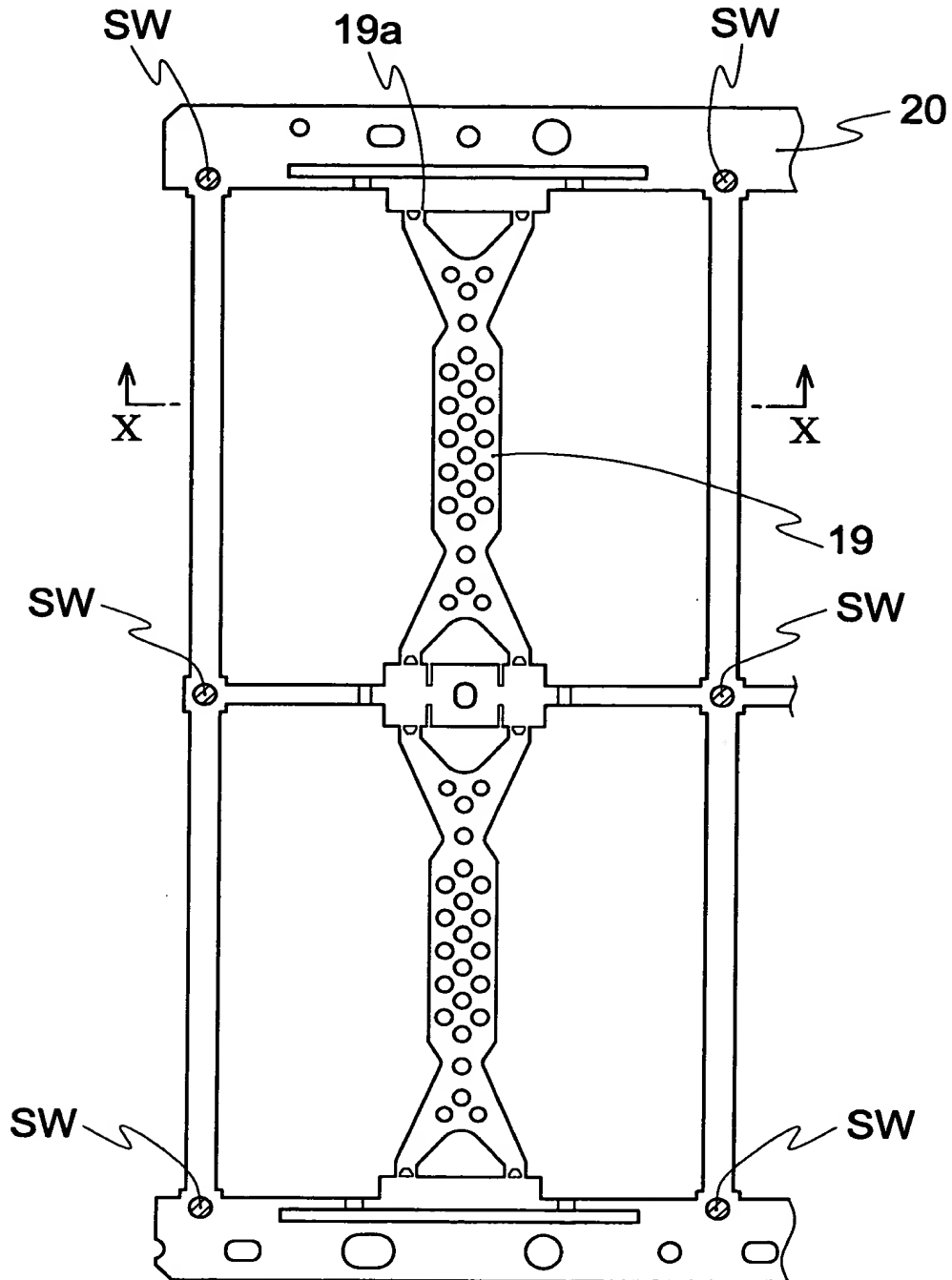


FIG. 10

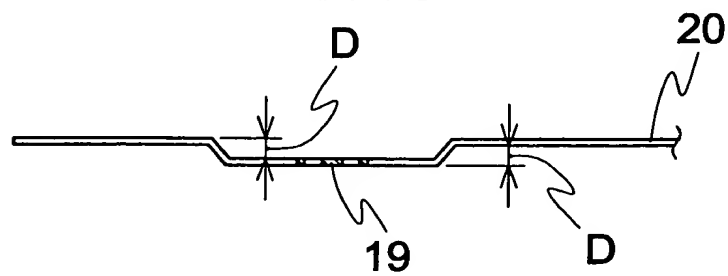


FIG. 11

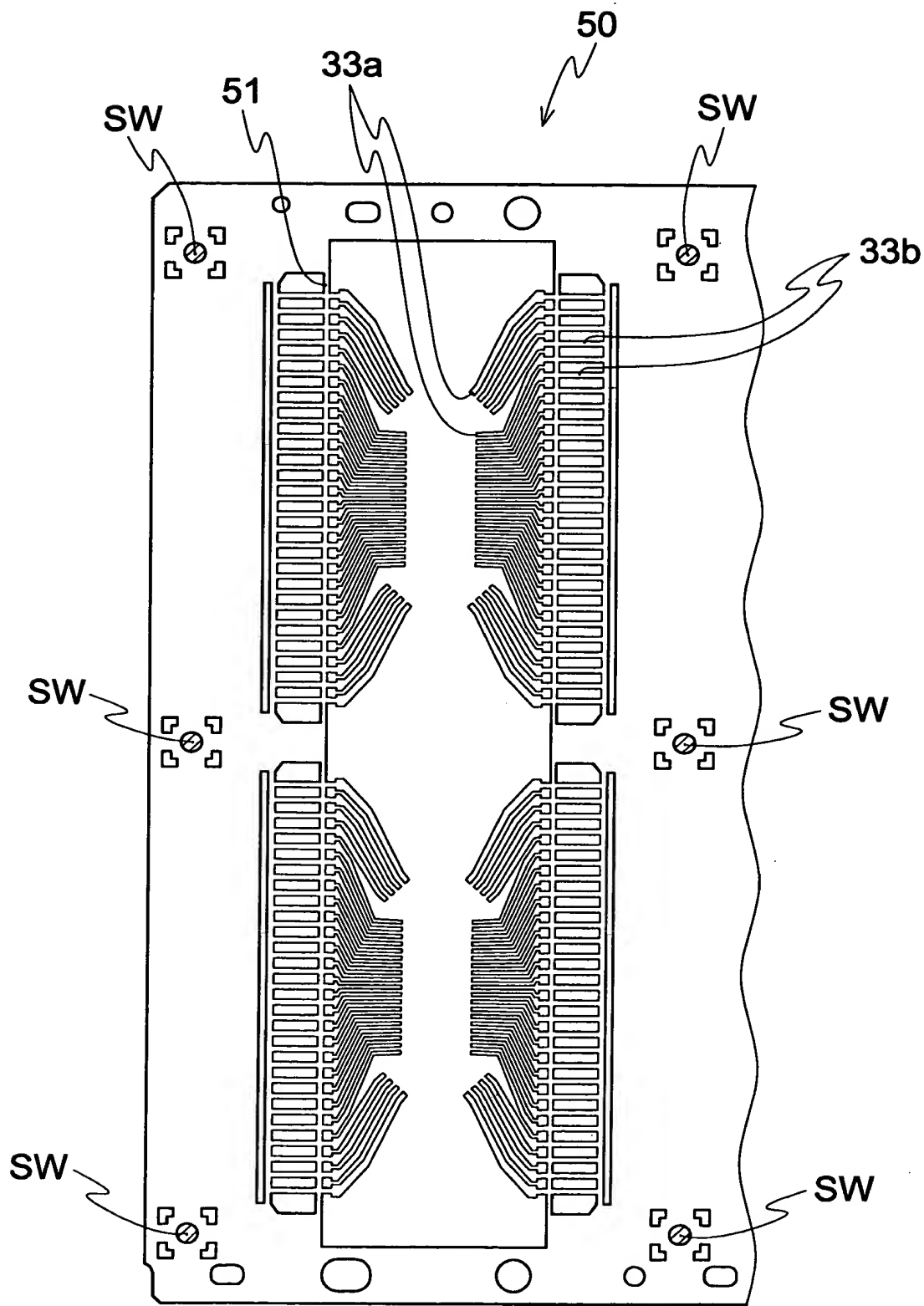


FIG. 11 is a schematic diagram of a semiconductor package 50. The package 50 is rectangular and contains two vertical columns of semiconductor elements, labeled 33a and 33b. Each column consists of multiple rows of elements, with each row having a central rectangular element and two side elements. The elements are interconnected by a network of lines. Six solder bumps, labeled SW, are positioned at the corners of the package. A label 51 points to a small circular feature at the top center. A label 33a points to the top of the left column, and a label 33b points to the top of the right column. The package is shown with a wavy line on its right side, indicating a cross-section or a specific layer.

FIG. 12

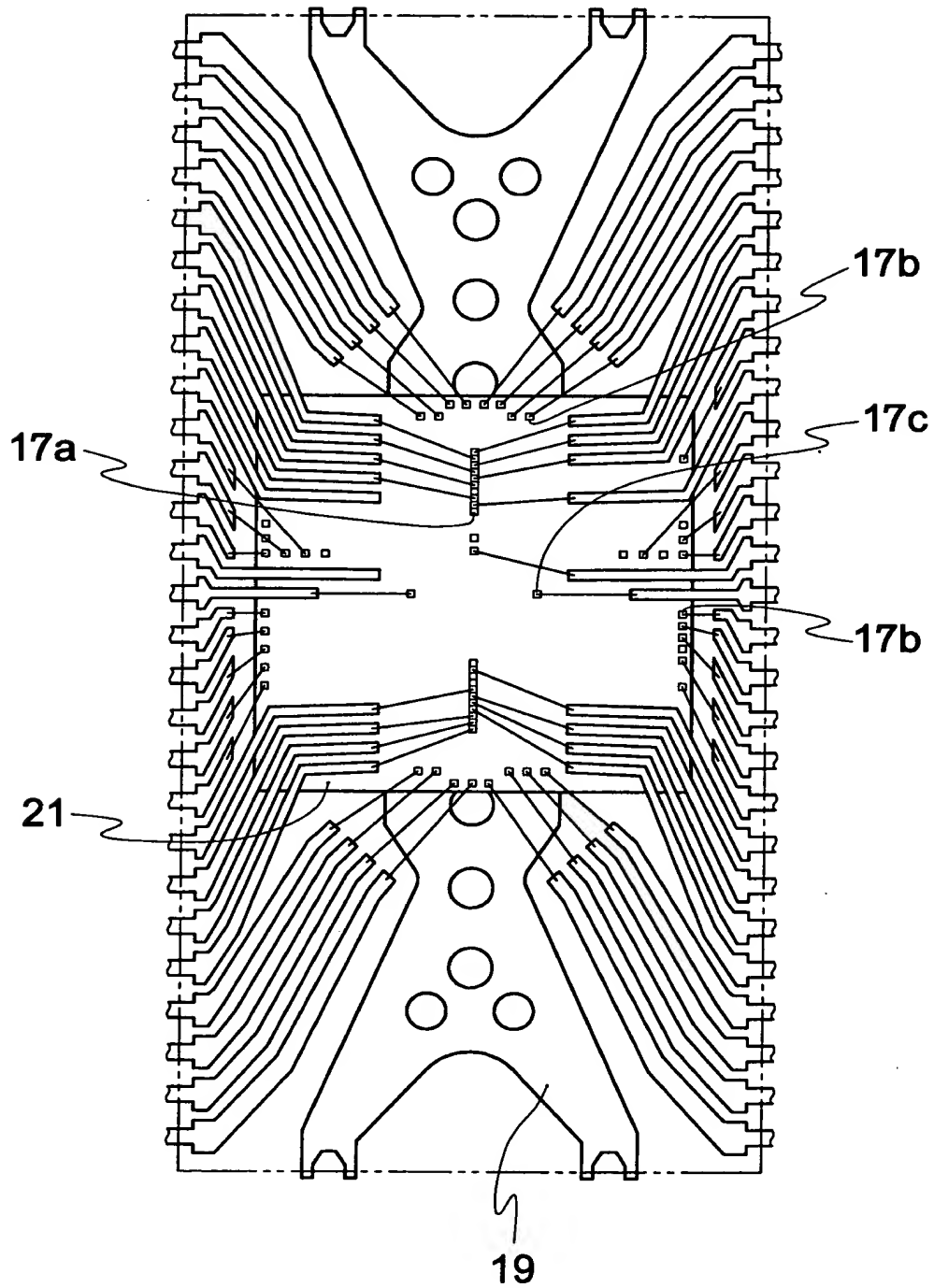


FIG. 13

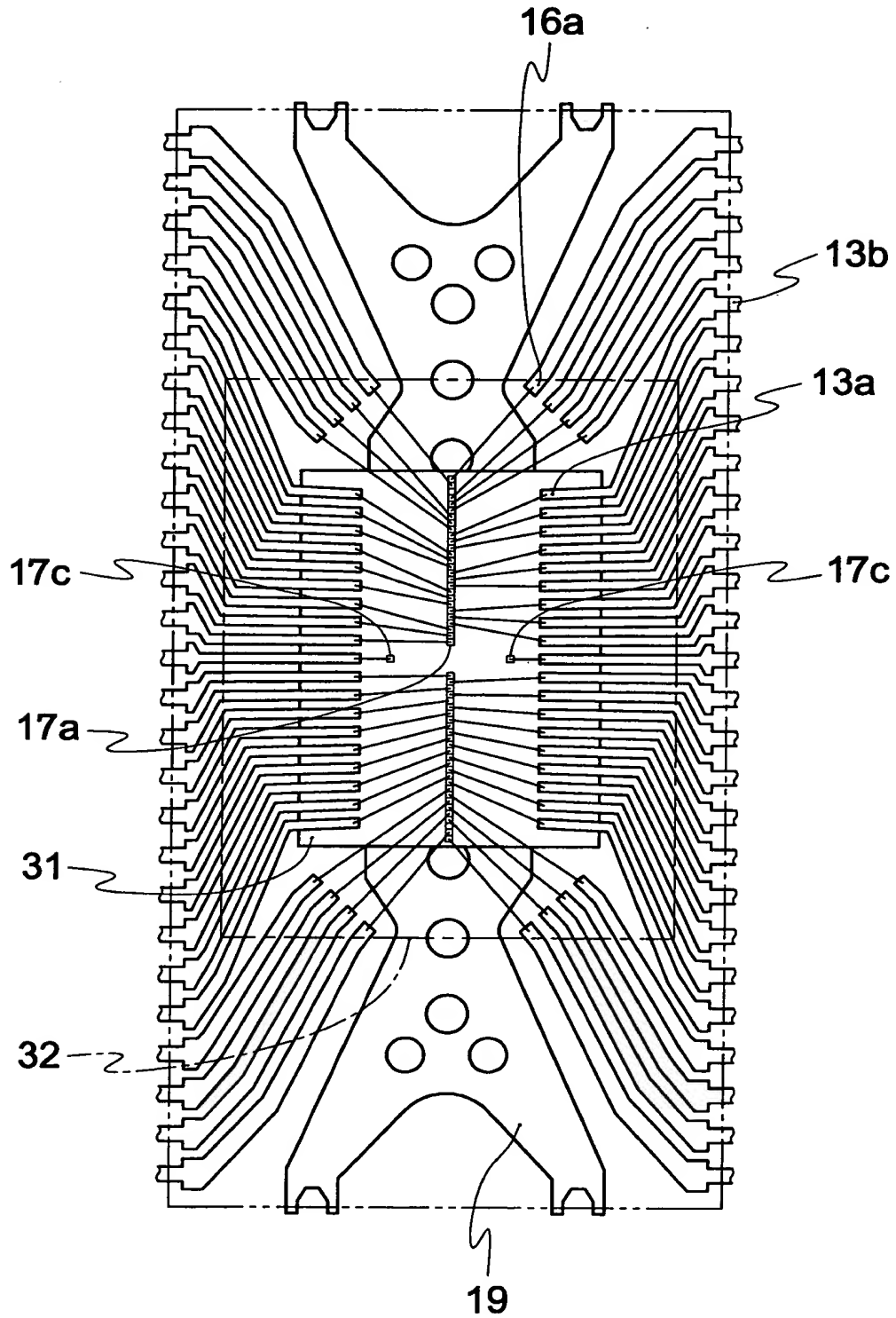




FIG. 14

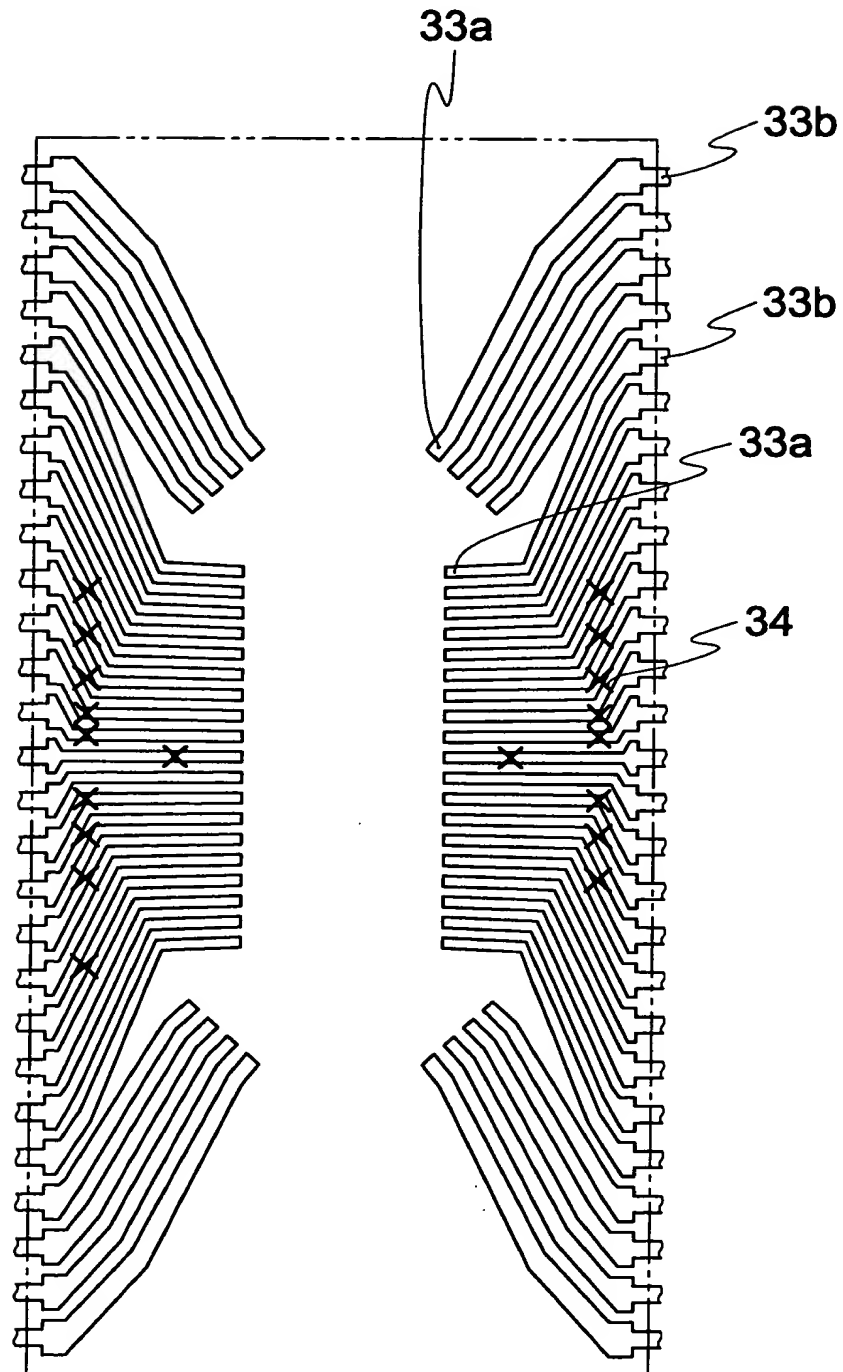


FIG. 15

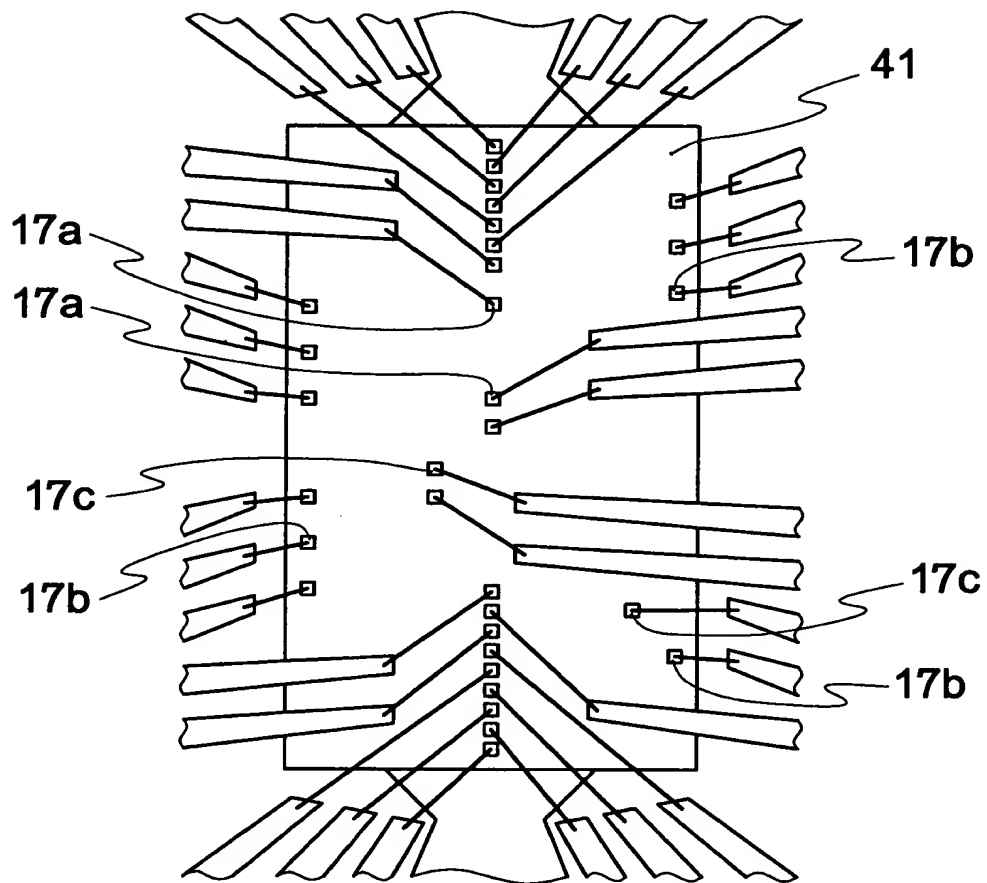


FIG. 16

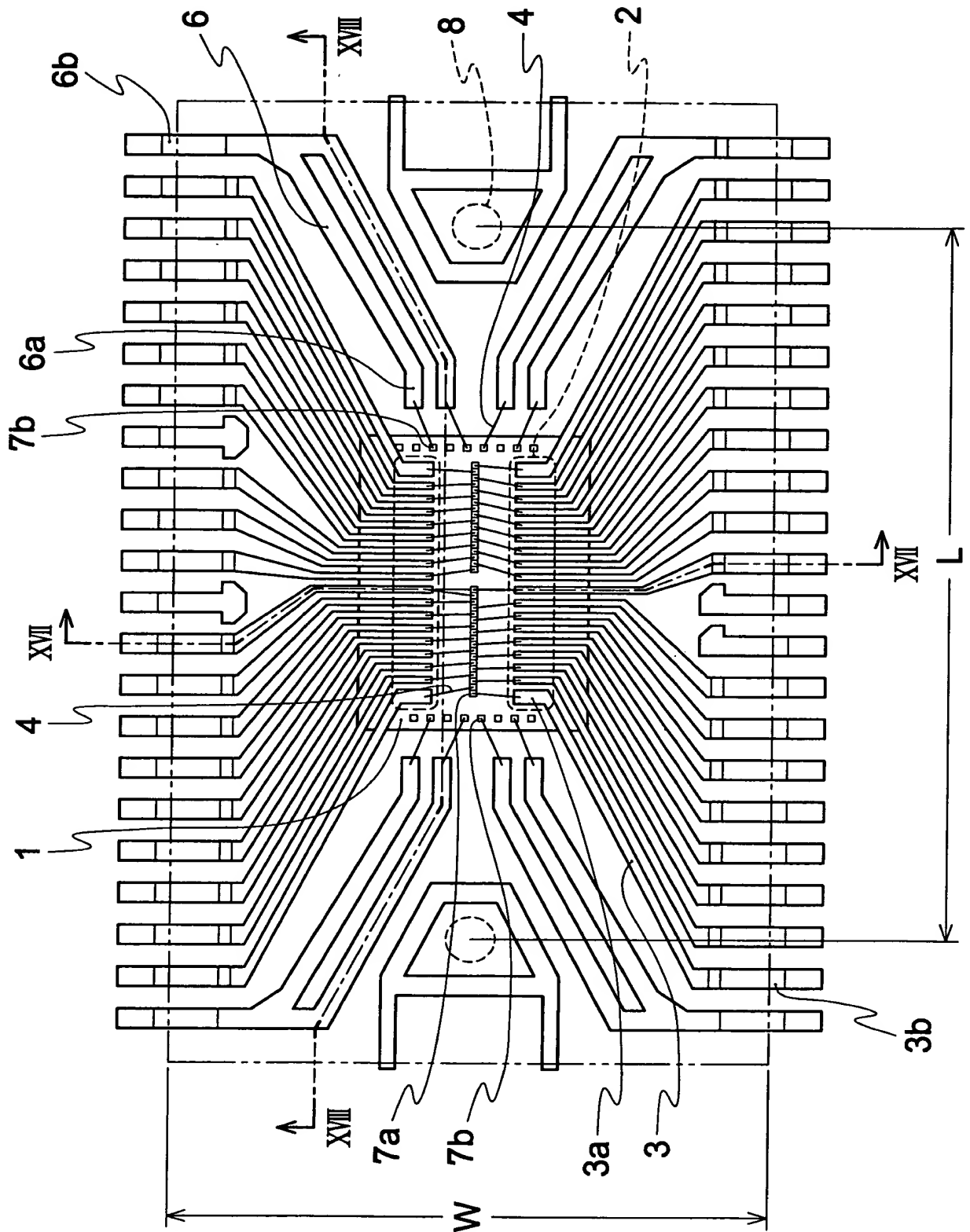


FIG. 18

